AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method of transmitting network data, the method comprising:

assembling the data into a data frame in a link layer implemented in programmable logic of an integrated circuit;

encapsulating the data frame into a data packet in a physical layer implemented in application-specific logic of the integrated circuit, the packet having a start field identifying the start of the packet and a data field including the data;

appending idle data to the data packet in the physical layer to form a packet assembly;

performing a cyclic redundancy check (CRC) of the data frame in the physical layer to obtain a CRC value; and

adding the CRC value to the data packet in the physical layer.

2. (Previously Presented) The method of claim 1, further comprising:

evaluating the packet assembly to obtain a disparity value; and

if the disparity value indicates an incorrect disparity, changing the packet assembly.

3. (Original) The method of claim 2, wherein changing the packet assembly comprises changing the idle data.

4. (Original) The method of claim 2, wherein the data packet includes an end-of-packet field, and wherein changing the packet assembly comprises changing the end-of-packet field.

5. (Original) The method of claim 1, wherein the idle data comprises a comma character.

6. (Original) The method of claim 5, wherein the comma character includes five consecutive identical bits.

7. (Original) The method of claim 6, wherein the five consecutive identical bits are logic zeros.

8. (Original) The method of claim 1, wherein appending the idle data occurs before performing the CRC of the data frame.

9. (Original) The method of claim 1, further comprising adding an extension field to the data frame before encapsulating the data into a data packet.

10. (Original) The method of claim 1, further comprising programming programmable logic to assemble the data frame.

11. (Original) The method of claim 10, wherein the programmable logic does not perform the CRC.

12. (Original) The method of claim 10, wherein the CRC is performed using application-specific logic.

13. (Previously Presented) A network physical layer coupled to transmit a data frame in a programmable logic device and instantiated in application-specific logic of the programmable logic device, the physical layer comprising:

a data node coupled to receive a data packet from a link layer implemented in programmable logic of the programmable logic device, the data packet including at least a portion of the data frame; and

a CRC generator coupled to the data node to perform a CRC on at least a portion of the data frame to provide a CRC value and to insert the CRC into the data packet.

14. (Previously Presented) The physical layer of claim 13, wherein the data node is further coupled to receive idle data.

15. (Previously Presented) The physical layer of claim 14, wherein the data packet and idle data collectively form a packet assembly, the physical layer further comprising an encoder coupled to receive the packet assembly and to provide a disparity value that is a function of the packet assembly.

16. (Previously Presented) The physical layer of claim 15, further comprising a packet-assembly modifier connected to the encoder and coupled to receive the disparity value and to modify the packet assembly in response to the disparity value.

17. (Previously Presented) The physical layer of claim 16, wherein the packet-assembly modifier outputs a modified packet assembly having modified idle data.

18. (Original) The physical layer of claim 16, wherein the disparity value may be positive or negative.

19. (Original) The physical layer of claim 18, wherein the packet-assembly modifier modifies the idle data in response to the positive disparity value.

20. (Original) The physical layer of claim 18, wherein the packet-assembly modifier leaves unmodified the idle data in response to the negative disparity value.

21. (Previously Presented) The physical layer of claim 13, wherein the CRC generator further comprises a first module enabling a first communication standard and a second module enabling a second communication standard.

22. (Original) The physical layer of claim 13, wherein the CRC generator further comprises a force-error input terminal.

23. (Previously Presented) The physical layer of claim 22, wherein the force-error input terminal is coupled to receive a test signal for inducing the CRC generator to produce an error.

24. (Previously Presented) A programmable logic device comprising:

an array of configurable logic blocks comprising a link layer implemented in programmable logic for transmitting network data; and

a network physical layer instantiated in hard logic and coupled to receive network data from the link layer;

wherein the physical layer comprises at least one CRC generator performing a cyclic redundancy check.

25. (Previously Presented) The programmable logic device of claim 24, wherein the CRC generator performs a plurality of CRC functions to support a plurality of communication standards.

26. (Previously Presented) The programmable logic device of claim 24, further comprising a data encapsulator coupled to receive a data frame and provide a data packet based on the data frame, wherein the CRC generator performs a CRC on at least a portion of the data frame to obtain a CRC value and to insert the CRC value into the data packet.

27. (Previously Presented) The programmable logic device of claim 26, wherein the data encapsulator adds idle data to the packet to form a packet assembly, the programmable logic device further comprising a packet-assembly modifier coupled to modify the packet assembly based in part on the CRC value.

28. (Original) The programmable logic device of claim 27, wherein the packet-assembly modifier modifies the idle data.

29. (Original) The programmable logic device of claim 24, wherein the at least one CRC generator further comprises a force-error input terminal.

30. (Previously Presented) The programmable logic device of claim 29, wherein

the force-error input terminal is coupled to receive a test signal for inducing the CRC generator to produce an error.

31. (Previously Presented) A network receiver coupled to receive data and instantiated in application-specific logic of a programmable logic device, the network receiver comprising a physical layer having a data node coupled to receive a packet assembly from a link layer implemented in programmable logic of the programmable logic device, the packet assembly including at least a portion of the data, and a CRC generator, wherein the CRC generator performs a CRC on at least a portion of the packet assembly to provide a calculated CRC value.

32. (Previously Presented) The network receiver of claim 31, wherein the packet includes a packet CRC value, the physical layer further comprising a CRC compare circuit comparing the packet CRC value to the calculated CRC value

33. (Previously Presented) The network receiver of claim 32, wherein the link layer is connected to the CRC compare circuit.

34. (Original) The network receiver of claim 33, wherein the CRC compare circuit of the physical layer identifies mismatches between the packet CRC and the calculated CRC for the link layer.

35. (Previously Presented) The network receiver of claim 33, wherein the link layer rejects defective packets, and wherein the link layer relies upon the CRC compare circuit in the physical layer to identify the defective packets.

36. (Previously Presented) The network receiver of claim 31 wherein the CRC generator performs a plurality of CRC functions to support a plurality of communication standards.

37. (Previously Presented) A system, comprising:

a network; and

a transmitter coupled to the network and transmitting a data frame to the network, the transmitter comprising a physical layer implemented in hard logic and a link layer implemented using programmable logic, the link layer being coupled between the physical layer and the network, the physical layer comprising:

a data node coupled to receive a data packet, the data packet including at least a portion of the data frame; and

a CRC generator coupled to the data node to perform a CRC on at least a portion of the data frame to provide a CRC value and to insert the CRC into the data packet.

38. (Original) The system of Claim 37, wherein the link layer and the physical layer of the transmitter each comprise portions of a programmable logic device (PLD).

39. (Original) The system of Claim 38, wherein the PLD is a field programmable gate array (FPGA).

40. (Previously Presented) The system of Claim 37, further comprising:

a receiver coupled to the network and coupled to receive data from the network, the receiver being implemented in hard logic, the receiver having a physical layer comprising:

a data node coupled to receive a packet assembly from the network, the packet assembly including at least a portion of the data; and

a CRC generator coupled to the data node to perform a CRC on at least a portion of the packet assembly to provide a calculated CRC value.

41. (Original) The system of Claim 40, wherein the link layer and the physical layer of the transmitter, and the physical layer and CRC generator of the receiver, each comprise portions of a programmable logic device (PLD).

42. (Original) The system of Claim 41, wherein the PLD is a field programmable

gate array (FPGA).

43. (Previously Presented) A system, comprising:

a network; and

a receiver coupled to the network to receive data from the network, the receiver being implemented in a programmable logic device, the receiver comprising:

a data node coupled to receive a packet assembly from the network, the packet assembly including at least a portion of the data and having a CRC generator coupled to the data node to perform a CRC on at least a portion of the packet assembly to provide a calculated CRC value, the data node and the CRC generator implemented in hard logic; and

a link layer implemented in programmable logic of the programmable logic device.

44. (Original) The system of Claim 43, wherein the physical layer and CRC generator of the receiver each comprise portions of a programmable logic device (PLD).

45. (Original) The system of Claim 44, wherein the PLD is a field programmable gate array (FPGA).